CLAIMS

What is claimed is:

1. A process for asymmetrically shrinking a layout for a VLSI circuit design, comprising:

   asymmetrically scaling a first VLSI circuit design layout defined by a first fabrication process, having first design rules, to a second VLSI circuit design layout defined by a second fabrication process, having second design rules; and

   processing layouts of one or more leaf cells of the second VLSI circuit design layout to ensure conformity to the second design rules.

2. The process of claim 1, the step of asymmetrical scaling further comprising reorienting one or more transistors in accord with the second design rules.

3. The process of claim 1, the step of asymmetrically scaling further comprising maintaining one or more port instance locations within the second VLSI circuit design layout relative to the first VLSI circuit design layout.

4. The process of claim 1, the step of processing further comprising processing via arrays of the second VLSI circuit design layout to conform to the second design rules.

5. The process of claim 1, the step of processing further comprising verifying hierarchy associated with the second VLSI circuit design layout.

6. The process of claim 1, the step of asymmetrically scaling further comprising symmetrically scaling design elements of the first VLSI circuit design layout according to the second design rules.

7. The process of claim 1, further comprising maintaining locations of port instances relative to the asymmetric scaling between the first VLSI circuit design layout and the second VLSI circuit design layout.

8. A software product comprising instructions, stored on computer-readable media, wherein the instructions, when executed by a computer, perform steps for asymmetrically shrinking a layout for a VLSI circuit design, comprising:

instructions for asymmetrically scaling a first VLSI circuit design layout, defined by a first fabrication process having first design rules, to a second VLSI circuit design layout, defined by a second fabrication process having second design rules; and

instructions for processing layouts of one or more leaf cells of the second VLSI circuit design layout to ensure conformity to the second design rules.

9. The software product of claim 8, the instructions for asymmetrical scaling further comprising instructions for reorienting one or more transistors in accord with the second design rules.

10. The software product of claim 8, the instructions for asymmetrical scaling further comprising instructions for maintaining one or more port instance locations within the second VLSI circuit design layout relative to the first VLSI circuit design layout.

11. The software product of claim 8, the instructions for processing further comprising instructions for processing via arrays of the second VLSI circuit design layout to conform to the second design rules.

12. The software product of claim 8, the instructions for processing further comprising instructions for verifying hierarchy associated with the second VLSI circuit design layout.

13. The software product of claim 8, the instructions for asymmetrically scaling further comprising instructions for symmetrically scaling design elements of the first VLSI circuit design layout according to the second design rules.

14. The software product of claim 8, further comprising instructions for maintaining locations of port instances relative to the asymmetric scaling between the first VLSI circuit design layout and the second VLSI circuit design layout.

15. A system for asymmetrically shrinking a layout for a VLSI circuit design, comprising:

means for asymmetrically scaling a first VLSI circuit design layout, defined by a first fabrication process having first design rules, to a second VLSI circuit design layout, defined by a second fabrication process having second design rules; and

means for processing layouts of one or more leaf cells of the second VLSI circuit design layout to ensure conformity to the second design rules.

16. The system of claim 15, the means for asymmetrically scaling comprising a layout update tool.

17. The system of claim 15, the means for asymmetrically scaling comprising means for maintaining one or more port instance locations within the second VLSI circuit design layout relative to the first VLSI circuit design layout.

18. The system of claim 15, the means for processing comprising means for verifying hierarchy associated with the second VLSI circuit design layout.